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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/244,270	02/03/1999	LORDSON L. YUE	M-7019-US	3568

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EXAMINER	
CHUNG, DANIEL J	
ART UNIT	PAPER NUMBER
2672	

DATE MAILED: 06/19/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/244,270	YUE ET AL.	
	Examiner	Art Unit	
	Daniel J Chung	2672	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 March 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 14-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 14-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *12* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claims 1-3 and 14-27 are presented for examination. This office action is in response to the Amendment filed on 3-27-2002.

The objection to the drawing has been withdrawn because of amendment.

Receipt is acknowledged of Applicant's Information Disclosure Statement of 4-29-2002, which has been placed in the application file and considered by the Examiner.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3 and 14-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aleksic (5,914,722) in view of Lentz et al (5,446,836) and Sfarti (5,528,737), and further in view of Wong et al (6,034,699).

Regarding claim 1, Aleksic discloses that the claimed feature of a method (See Fig 2, Fig 4A-4B, col 2 line 65-col 3 line 27) comprising:

Receiving vertex data corresponding to the vertices of a primitive, the vertex data including x-coordinate and y-coordinate position information (See Fig 2, col 2 line 24-28)

Sorting the vertex data in coordinate dependent fashion (See Fig 2, Fig 4A, Fig 4B, col 2 line 54-59, col 2 line 65-col 3 line 27, col 4 line 55+; Also See Fig 9-11, col 5 line 31-col 6 line 67 in Wong et al)

Generating region bits representing the location of the sorted vertex data with respect to a current tile [17;a memory page] being rendered (See Fig 2, Fig 4A, Fig 4B, col 2 line 54-59, col 2 line 65-col 3 line 27, col 4 line 55+)

Generating coordinate data representing an initial rasterization starting point estimate when the region bits indicate that at least one of the sorted vertex data lies within the current tile being rendered and discarding the sorted vertex data of primitives that lie outside the boundary of the current tile being rendered. (See Fig 2, Fig 4A, Fig 4B, col 2 line 54-59, col 2 line 65-col 3 line 27, col 4 line 55+)

Providing the initial rasterization starting point estimate to a rasterizer. (See Fig 2, Fig 4A, Fig 4B, col 2 line 54-59, col 2 line 65-col 3 line 27, col 4 line 55+)

Aleksic does not specifically disclose that the estimated rasterization starting point. However, Lentz et al teaches that the method of finding[step 1110 in Fig 11A] the starting raster points[X mark in Fig 9] by using the vertices of the polygon. (See Fig 2, Fig 4A, Fig 4B, Fig 5, Fig 6, Fig 10, Fig 11A-B, col 3 line 36-col 4 line 46, col 5 line 29-col 6 line 4) The motivation would have been to decreasing a substantial time of the rasterization efficiently and to minimize computation time for rasterization, as mentioned in Lentz et al (See col 3 line 36-col 4 line 46, col 5 line 19-21). Therefore, it would have

been obvious to one skilled in the art to incorporate the teaching of Lentz et al into the teaching of Aleksic.

Aleksic does not explicitly disclose the step of sorting the vertex data. However, Sfarti teaches such claimed feature of invention. (See Abstract, Fig 4, col 3 line 46-63, col 7 line 11-13) The motivation would have been to minimize computation by easily determining the edges bound, as mentioned by Sfarti. (See col 3 line 54-55) Therefore, it would have been obvious to one skilled in the art to have sorting step into the teaching of Aleksic.

Also, Aleksic does not explicitly disclose that "generating an initial rasterization starting point based on the region bits." However, Wong et al discloses that the determining the initial starting point of the scanning process [in the step of "rasterization"] based on the angular orientation of the edge ["the region bits"] of the polygon. (See Abstract, Fig 7, Fig 9-10, Fig 11-13, Fig 15, col 2 line 27-col 3 line 51, col 4 line 33-49, col 5 line 31-col 7 line 34, col 7 line 55-col 8 line 44) The motivation would have been to minimized the time required to scan/render the polygon, as mentioned in Wong et al. (See col 2 line 62-64) Therefore, it would have been obvious to one skilled in the art to incorporate the teaching of Wong et al into the teaching of Aleksic.

Regarding claim 2, Aleksic discloses that generating an orientation bit representing an orientation of a line connecting the first and second vertices of the sorted primitive with respect to a line connecting the first and third vertices of the sorted primitive before generating the initial rasterization starting point coordinates. (See Fig 2, Fig 4A, Fig 4B, col 2 line 54-59, col 2 line 65-col 3 line 27, col 4 line 55+; also See col 1 line 58-67 in Sfarti)

Aleksic does not explicitly disclose that representation of orientation bit. However, Lentz et al teaches that using orientation of triangles to classify or organize the triangle variable for faster and easier rasterization process. (See col 5 line 58-64, col 7 line 38-51) The motivation would have been to improve faster rasterization process by providing the x-y coordinate data of each vertex in different coordinate system with easy manner. Furthermore, calculating an orientation of two side of a triangle is necessarily required for classifying the triangle base on its shape [i.e. right oriented triangle, left oriented triangle] in order to render/raster the triangle/primitives effectively with easy manner. Therefore, it would have been obvious to one skilled in the art to have orientation bit into the teaching of Aleksic.

Regarding claim 3, Aleksic discloses that sorting the first, second and third vertices according to a position in a predetermined direction. (See Fig 2, Fig 4A, Fig 4B,

col 2 line 54-59, col 2 line 65-col 3 line 27, col 4 line 55+; Also See Fig 9-11, col 5 line 31-col 6 line 67 in Wong et al)

Regarding claim 14, claim 14 is similar in scope to the claim 4, and thus the rejection to claim 4 hereinabove is also applicable to claim 14.

Regarding claim 15, refer to the discussion for the claim 1 hereinabove, Wong et al discloses that the initial rasterization starting point estimation circuit includes a trivial accept circuit operative to provide the initial rasterization starting point in response to the region bits. (See Abstract, Fig 7, Fig 13, col 2 line 47-col 3 line 51)

Regarding claim 16, refer to the discussion for the claim 1 hereinabove, Wong et al discloses that the vertex data is sorted in y-coordinate fashion and the trivial accept circuit provides the x-coordinate and sorted y-coordinate rasterization starting point of a non-discarded primitive. (See Abstract, Fig 7, Fig 13, col 2 line 47-col 3 line 51)

Regarding claim 17, refer to the discussion for the claim 1 hereinabove, Wong et al discloses that an interception calculation circuit operative to provide a coordinate dependent initial rasterization starting point in response to the region bits and the vertex data. (See Abstract, Fig 7, Fig 13, col 2 line 47-col 3 line 51)

Regarding claim 18, refer to the discussion for the claim 1 hereinabove, Wong et al discloses that the boundary interception point generated by the intercept calculation circuit represents the initial rasterization point starting point coordinate. (See Abstract, Fig 7, Fig 13, col 2 line 47-col 3 line 51)

Regarding claim 19, refer to the discussion for the claim 1 hereinabove, Wong et al discloses that an interception calculation circuit operative to provide a coordinate dependent initial rasterization starting point in response to the region bits and the sorted vertex data. (See Abstract, Fig 7, Fig 13, col 2 line 47-col 3 line 51)

Regarding claim 20, refer to the discussion for the claim 1 hereinabove, Wong et al discloses that the trivial accept circuit comprises a logic gate coupled to a corresponding subset of the region bits. (See Fig 7, 13, 9-10, 15)

Wong et al does not disclose that "logic gate". However, logic gate is inherent by the any image processing circuitry, in order to produce any arithmetic calculation in image processing system. Therefore, it would have been obvious to one skilled in the art to include the logic gate into the teaching of Aleksic.

Regarding claim 21, refer to the discussion for the claim 1 hereinabove, Wong et al discloses that the logic gate is an AND gate. (See Fig 7, 13, 9-10, 15)

Regarding claim 22, refer to the discussion for the claim 1 hereinabove, Wong et al discloses that the region bits define the top edge, bottom edge, right edge and left edge of a current tile being rendered. (See Fig 9, 10, 11-12, col 2 line 5-25)

Regarding claim 23, refer to the discussion for the claim 1 hereinabove, Wong et al discloses that a first AND gate having an output and inputs coupled to data representing the right most boundary of the current tile being rendered; a second AND gate having an output and inputs coupled to data representing the left most boundary of the current tile being rendered; and an OR gate having a first input coupled to the output of the first AND gate, a second input coupled to the output of the second AND gate, a third input coupled to data representing the top most boundary of the current tile and a fourth input coupled to data representing the bottom most boundary of the current tile, wherein the output of the OR gate provides a signal indicating whether the sorted vertex data lies within the current tile being rendered. (See Fig 9, 10, 11-12, col 2 line 5-25)

Regarding claim 24, refer to the discussion for the claim 1 hereinabove, Wong et al discloses that the x-coordinate and y-coordinate of the initial rasterization starting point to the boundary intercept points. (See Abstract, Fig 7, Fig 13, col 2 line 47-col 3 line 51)

Regarding claim 25, refer to the discussion for the claim 1 hereinabove, Lentz et al discloses that generating an orientation bit representing an orientation of a line connecting the sorted first and second vertices with respect to a line connecting the sorted first and third vertices. (See col 5 line 58-64, col 7 line 38-51; also See col 1 line 58-67 in Sfarti)

Regarding claim 26, refer to the discussion for the claim 1 hereinabove, Lentz et al discloses that determining the relative positioning between the vertices of the primitive. (See col 5 line 58-64, col 7 line 38-51; also See col 1 line 58-67 in Sfarti)

Regarding claim 27, claim 27 is similar in scope to the claim 1, and thus the rejection to claim 1 hereinabove is also applicable to claim 27.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1-3 and 14-27 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 2 and 4-15 of co-pending Application No. 09/244,265. Although the conflicting claims are not identical, they are not patentably distinct from each other because both applications have same scopes of the claims.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Response to Amendment/Argument

Applicant's arguments with respect to claims 1-3 and 14-27 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel J. Chung whose telephone number is (703) 306-3419. He can normally be reached Monday-Thursday

and alternate Fridays from 7:30am- 5:00pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael, Razavi, can be reached at (703) 305-4713.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

djc
June 14, 2002

MATTHEW LUU
PRIMARY EXAMINER